Amendment to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application. The following listing provides the amended claims with the amendments marked with deleted material crossed out and new material underlined to show the changes made.

Claims 1-27 (Canceled).

28. (Original) For an electronic-design-automation placer that uses a set of partitioning lines, that define a plurality of slots, to partition an integrated-circuit ("IC") layout region into a plurality of sub-regions corresponding to said slots, a method of pre-computing placement costs for multiple wiring models, the method comprising:

a) for each combination of said slots, identifying at least one connection graph that is based on a first wiring model and that represents the topology of interconnect lines necessary for connecting the combination of said slots according to the first wiring model;

b) for each combination of said slots, identifying at least one connection graph that is based on a second wiring model and that represents the topology of interconnect lines necessary for connecting the combination of said slots according to the second wiring model;

c) computing an attribute of each identified connection graph; and

d) storing the computed attributes in a storage structure.

29. (Original) The method of claim 28, wherein the connection graphs are Steiner trees.

30. (Original) The method of claim 28, wherein the connection graphs are minimum spanning trees.

31. (Original) The method of claim 28, wherein computing said attribute comprises calculating the length of each graph.

32. (Original) The method of claim 28, wherein computing said attribute comprises calculating the number of bends in each graph.

33. (Original) The method of claim 32, wherein the bends are diagonal bends.

34. (Original) The method of claim 28, wherein a plurality of interconnect-line paths exist between said slots, wherein computing the attribute comprises identifying the interconnect line paths used by each connection graph.

35. (Original) The method of claim 34, wherein a first set of interconnect-line paths exist between said slots when the first wiring model is used, and a second set of interconnect-line paths exist between said slots when the second wiring model is used.

36. (Currently Amended) The method of claim 28, wherein a plurality of edges exist between said slots, wherein computing the ~~first~~ attribute comprises identifying the edges intersected by each connection graph.

37. (Original) The method of claim 36, wherein a first set of edges exist between said slots when the first wiring model is used, and a second set of edges exist between said slots when the second wiring model is used.

38. (Currently Amended) A method of placing circuit modules in a region of an integrated circuit ("IC") layout, said IC layout having a plurality of circuit elements, wherein a plurality of nets represent interconnections between said circuit elements, each net defined to include a set of circuit elements, the method comprising:

a) selecting a first wiring model from ~~among~~ a ~~plurality~~ set of at least two wiring models, each wiring model providing a wiring direction for each layer of said IC layout, wherein the first wiring model includes a wiring direction that is not available on any layer of at least one other wiring model in the set of wiring models~~each wiring model specifying different types of interconnect lines~~;

b) partitioning the IC region into several sub-regions;

c) selecting a net;

d) identifying the set of sub-regions containing the circuit elements of the selected net;

e) retrieving, from a storage structure, a pre-computed attribute of a set of one or more interconnect lines that are necessary for connecting the identified set of sub-regions, wherein said set of interconnect lines are based on the first wiring model.

39. (Previously Presented) The method of claim 38, wherein the retrieved attribute represents the placement cost of said net within said region.

40. (PreviouslyPresented) The method of claim 38 further comprising computing the placement cost of said net from said retrieved attribute.

41. (Currently Amended) The method of claim 38 further comprising:

fa) changing the position of a circuit element of the net from one sub-region to another;

gb) identifying a new set of sub-regions that contain the circuit elements of the net;

hc) retrieving, from the storage structure, a pre-computed attribute of a different set of interconnect lines necessary for connecting the identified new set of sub-regions, wherein said different set of interconnect lines are based on the first wiring model.

42. (Currently Amended) A method of placing circuit modules in a region of an integrated circuit ("IC") layout, said IC layout having a plurality of circuit elements, wherein a plurality of nets represent interconnections between said circuit elements, each net defined to include a set of circuit elements, the method comprising:

a) selecting a first wiring model from ~~among~~ a ~~plurality~~ set of at least two wiring models, each wiring model providing a wiring direction for each layer of said IC layout, wherein the first wiring model includes a wiring direction that is not available on any layer of at least one other wiring model in the set of wiring models~~each wiring model specifying different types of interconnect lines~~;

b) partitioning the IC-layout region into several sub-regions;

c) for each particular net, identifying the set of sub-regions containing the circuit elements of the particular net,

d) for each particular net, retrieving a pre-computed attribute of a connection graph that is based on the first wiring model, and that represents the topology of interconnect lines needed to connect the identified set of sub-regions of the particular net;

e) computing a placement cost for the IC layout within said region by using the retrieved attributes.

43. (Currently Amended) The method of claim 42 further comprising:

fa) changing the position of a particular circuit element from one sub-region to another;

gb) for each particular net that includes the particular circuit element, identifying a new set of sub-regions that contain the circuit elements of the particular net;

hc) for each particular net that includes the particular circuit element, retrieving a pre-computed attribute of a new connection graph that is based on the first wiring model, and that represents the topology of interconnect lines necessary for connecting the identified new set of sub-regions for the particular net;

id) computing a delta placement cost based on the retrieved attributes of the new connection graphs.

44. (Original) The method of claim 42, wherein the connection graphs are Steiner trees.

45. (Original) The method of claim 42, wherein the connection graphs are minimum spanning trees.